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FROM: **Albert C. Metrailer (sent by Karen Harris)**

DATE: **December 21, 2004**

RE: U.S. Patent Application Serial No. 09/745,919
Filing Date: December 21, 2000
Atty Docket IDF 1501 (4000-02700)
Notification of Non-Compliance Second Corrected Appeal Brief (30 pages)
U.S. Patent No. 5,592,509 (11 pages)
Transmittal Cover Sheet (1 page)

Total Number of Pages (Including Cover Page): 43

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	42

Application Number	09/745,919
Filing Date	December 21, 2000
First Named Inventor	Thomas R. Bayerl
Group Art Unit	2181
Examiner Name	Dang, Khanh NMN
Attorney Docket Number	IDF 1501 (4000-02700)

ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
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  - ☐ Affidavits/declaration(s)
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  - **Transmittal Cover Sheet**
  - **U.S. Patent 5,592,509**

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

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Atty. Dkt. No. IDF 1501 (4000-02700)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Thomas R. Bayerl, et al.	§	
		§	Group Art Unit: 2181
Serial No.:	09/745,919	§	
		§	Examiner: Dang, Khanh NMN
Filed:	December 21, 2000	§	
		§	Confirmation No.: 6827
For:	Use of Bus Hold to Prevent Bus Contention Between High Speed Processor and Slow Peripheral	§	

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Karen A. Harris
Karen A. Harris

NOTIFICATION OF NON-COMPLIANCE
SECOND CORRECTED APPEAL BRIEF

Dear Sirs:

In response to the Notice of Non-Compliance dated November 24, 2004, having a shortened statutory period for response which expires on December 24, 2004, and the Interview Summary mailed December 7, 2004, the Applicants hereby resubmit the following second corrected Appeal Brief originally filed on June 23, 2004. This paper was previously filed responsive to the Final Office Action

dated January 28, 2004, the Advisory Action dated April 8, 2004 and the Notice of Appeal filed May 3, 2004 in the above-styled matter.

Atty. Dkt. No. IDF 1501 (4000-02700)

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(I) REAL PARTY IN INTEREST

The real party in interest in this application is Sprint Communications Company L.P.

(II) RELATED APPEALS AND INTERFERENCES

None.

(III) STATUS OF CLAIMS

There are 12 Claims pending in the application. The 12 claims are reproduced in the Claims Appendix attached hereto. All 12 claims are under final rejection pursuant to the Final Office Action of January 28, 2004.

(IV) STATUS OF AMENDMENTS

A Response dated February 26, 2004 to the Final Office Action of January 28, 2004 was filed. The Advisory Action of March 8, 2004 indicates that proposed amendments would be entered for purposes of appeal. However, no amendments to the claims were made in the response to the Final Office Action.

(V) SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent Claim 1:

Claim 1 covers a method for preventing contention on a data bus connecting a central processing unit, CPU, and a peripheral device when the CPU performs a read operation followed by a write operation. (Page 7, lines 2-5; Page 11, lines 8-12;and preambles of original claims 1 and 5)

The first element: "connecting a transceiver with bus hold circuitry and an output enable input in the data bus between the central processing unit and the peripheral", is supported by Fig. 1 showing the data ports of a CPU 10 and an I/O Device 16, i.e. a peripheral, connected to sections 12 and 14 respectively of a common bus comprising the sections 12 and 14. (Page 8, lines 7-10) Bus sections 12 and 14 are connected to data ports of a transceiver circuit 18 having bus hold circuitry on its data ports and having an output enable, OE, control signal input connected to control signal line 36. (Page 8, lines 14-15 and page 9, lines 10-13)

The next element: "generating a control signal which ends at a preselected time before the end of the read operation" is supported by Fig. 1 where control logic unit 28 receives control signals 26, 30, 32, and 34 from the CPU 10 (page 9, lines 4-9) and provides control signals 36, 38 to the transceiver 18 (page 9, lines 10-13) and control signals 40, 42, 44 to the peripheral 16 (page 9, lines 17-20). Control logic 28 generates the OE signal coupled by signal line

36 to the OE input of the transceiver 18 using the control signals including the data strobe signal 32, DS, from the CPU 10 as explained in the second full paragraph of page 9 of the specification (page 9, lines 10-16). As shown in Fig. 2, the OE control signal is intentionally changed to a state at which the data output of the transceiver 18 would normally not be enabled before the end of the read operation, in this example about two clock cycles before. (Page 11, lines 20-22 and page 12, lines 1-2) This shortened OE signal 36 results from the shortened DS signal 32 produced by the CPU 10 as also shown in Fig. 2. (Page 11, lines 17-18)

The last element of Claim 1: "providing the control signal to an input of the peripheral and to the output enable input of the transceiver" is supported by Fig. 1 where control logic unit 28 receives control signals 26, 30, 32, and 34 from the CPU 10 (page 9, lines 4-9) and provides control signals 36, the OE signal, to the transceiver 18 (page 9, lines 10-13) and control signals 40, 42, 44 to the peripheral 16 (page 9, lines 17-20).

Independent Claim 5:

Claim 5 covers apparatus for preventing contention on a data bus connecting a central processing unit, CPU, and a peripheral device when the CPU performs a read operation followed by a write operation. (Page 7, lines 2-5; Page 11, lines 8-12;and preambles of original claims 1 and 5)

The first element: "a transceiver with bus hold circuitry and an output enable input connected between the data bus input/output connections of the central processing unit and the peripheral", is supported by Fig. 1 showing the data ports of a CPU 10 and an I/O Device 16, i.e. a peripheral, connected to sections 12 and 14 respectively of a common bus comprising the sections 12 and 14. (Page 8, lines 7-10) Bus sections 12 and 14 are connected to data ports of a transceiver circuit 18 having bus hold circuitry on its data ports and having an output enable, OE, control signal input connected to control signal line 36. (Page 8, lines 14-15 and page 9, lines 10-13)

The next element: "control logic having an input for receiving a CPU chip select signal and an output for providing a peripheral control signal which ends at a preselected time before the end of the read operation" is supported by Fig. 1 where control logic unit 28 receives control signals 26, 30, 32, and 34 from the CPU 10 (page 9, lines 4-9) and provides control signals 36, 38 to the transceiver 18 (page 9, lines 10-13) and control signals 40, 42, 44 to the peripheral 16 (page 9, lines 17-20). Control logic 28 generates the OE signal coupled by signal line 36 to the OE input of the transceiver 18 using the control signals including the data strobe signal 32, DS, from the CPU 10 as explained in the second full paragraph of page 9 of the specification (page 9, lines 10-16). As shown in Fig. 2, the OE control signal is intentionally changed to a state at which the data output of the transceiver 18 would normally not be enabled before the end of the

read operation, in this example about two clock cycles before. (Page 11, lines 20-22 and page 12, lines 1-2) This shortened OE signal 36 results from the shortened DS signal 32 produced by the CPU 10 as also shown in Fig. 2. (Page 11, lines 17-18)

The last element: "said control logic output connected to a control input of the peripheral and to the output enable input of the transceiver", is supported by Fig. 1 where control logic unit 28 receives control signals 26, 30, 32, and 34 from the CPU 10 (page 9, lines 4-9) and provides control signals 36, the OE signal, to the transceiver 18 (page 9, lines 10-13) and control signals 40, 42, 44 to the peripheral 16 (page 9, lines 17-20).

Independent claim 9:

Claim 9 covers a method for controlling the reading of data by a processing unit from a peripheral device over a bidirectional data bus during a read operation, said peripheral device having a maximum time to enable high impedance state. Page 6, lines 14-16; Page 6, line 23 to page 7, line 5

The first element: "connecting a transceiver with bus hold circuitry and an output enable input in the data bus between the central processing unit and the peripheral", is supported by Fig. 1 showing the data ports of a CPU 10 and an I/O Device 16, i.e. a peripheral, connected to sections 12 and 14 respectively of a common bus comprising the sections 12 and 14. (Page 8, lines 7-10) Bus

sections 12 and 14 are connected to data ports of a transceiver circuit 18 having bus hold circuitry on its data ports and having an output enable, OE, control signal input connected to control signal line 36. (Page 8, lines 14-15 and page 9, lines 10-13)

The second element: "generating a peripheral control signal which ends at a time equal to or greater than said maximum time to enable high impedance state before the end of the CPU read command" is supported by Fig. 1 where control logic unit 28 receives control signals 26, 30, 32 (the data strobe or DS signal), and 34 from the CPU 10 (page 9, lines 4-9) and provides control signals 36, 38 to the transceiver 18 (page 9, lines 10-13) and control signals 40, 42 (the data strobe or DS signal), 44 to the peripheral 16 (page 9, lines 17-20). The DS signal is shortened to instruct the peripheral to go to high impedance or tristate before the end of the read cycle to be sure it reaches that state before a write cycle can begin. See Fig. 2; page 7, lines 9-12; and page 11, lines 10-12

The last element "providing the peripheral control signal to an input of the peripheral and to the output enable input of the transceiver" is supported by Fig. 1 where control logic unit 28 receives control signals 26, 30, 32, and 34 from the CPU 10 (page 9, lines 4-9) and provides control signals 36, the OE signal, to the transceiver 18 (page 9, lines 10-13) and control signals 40, 42, 44 to the peripheral 16 (page 9, lines 17-20).

Independent claim 11:

Claim 11 covers apparatus for controlling the reading of data by a processing unit from a peripheral device over a bidirectional data bus during a CPU read operation, said peripheral device having a control input and a maximum time to enable high impedance state. Page 6, lines 14-16; Page 6, line 23 to page 7, line 5

The first element: "a transceiver with bus hold circuitry connected between the data bus input/output connections of the central processing unit and the peripheral, said transceiver having an output enable input", is supported by Fig. 1 showing the data ports of a CPU 10 and an I/O Device 16, i.e. a peripheral, connected to sections 12 and 14 respectively of a common bus comprising the sections 12 and 14. (Page 8, lines 7-10) Bus sections 12 and 14 are connected to data ports of a transceiver circuit 18 having bus hold circuitry on its data ports and having an output enable, OE, control signal input connected to control signal line 36. (Page 8, lines 14-15 and page 9, lines 10-13)

The second element: "control logic having an input for receiving a CPU data strobe signal and an output for providing a peripheral control signal which ends at a time equal to or greater than said maximum time to enable high impedance state before the end of the read operation" is supported by Fig. 1 where control logic unit 28 receives control signals 26, 30, 32 (the data strobe or DS signal), and 34 from the CPU 10 (page 9, lines 4-9) and provides control

signals 36, 38 to the transceiver 18 (page 9, lines 10-13) and control signals 40, 42 (the data strobe or DS signal), 44 to the peripheral 16 (page 9, lines 17-20). The DS signal is shortened to instruct the peripheral to go to high impedance or tristate before the end of the read cycle to be sure it reaches that state before a write cycle can begin. See Fig. 2; page 7, lines 9-12; and page 11, lines 10-12.

The last element "said control logic output connected to a control input of the peripheral and to the output enable input of the transceiver" is supported by Fig. 1 where control logic unit 28 receives control signals 26, 30, 32, and 34 from the CPU 10 (page 9, lines 4-9) and provides control signals 36, the OE signal, to the transceiver 18 (page 9, lines 10-13) and control signals 40, 42, 44 to the peripheral 16 (page 9, lines 17-20).

(VI) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-3,5-7, 9, and 11 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 5,592,509, McClear et al.

Claims 4, 8, 10, and 12 stand rejected under 35 U.S.C. §103(a) as being obvious in view of U.S. Patent 5,592,509, McClear et al.

(VII) ARGUMENT

Argument re 102 rejections:

Claims 1-3, 5-7, 9, and 11 were finally rejected under 35 U.S.C. §102(b) over McClear et al. U.S. Patent 5,592,509. The basic rejection was that "these claims do not define any structure/step that differs from McClear et al."

The McClear reference with reference to its Fig. 1, describes at Col. 1, lines 18-43, and Col. 2, line 44 through Col. 3, line 7 a prior art transceiver which is equivalent to the transceiver 18 of the present invention. McClear notes at Col. 1, lines 22-25, that the prior art transceiver has direction and output enable control lines. McClear distinguishes its invention at Col.1, lines 51-55 as a "...transceiver ... **without control lines** from the processor to the transceiver.' and at Col. 2, lines 7-9, "...provides drive to an output **without the need for enable or control lines**." The transceiver of McClear has no control lines from or to the processor. Since the device of McClear has no output enable control line input, it cannot receive an output enable input, much less an output enable input which ends before the end of a read operation.

With regard to Claims 5 and 11, the Examiner has asserted that McClear: provides apparatus for preventing contention on a data bus connecting a central processing unit and a peripheral device when the central processing unit calls for a read operation followed by a write operation, comprising; a transceiver (83, for example) with bus hold circuitry (see at least Fig. 3) and an output enable input

(see at least Fig. 2 and discussion provided below) connected between the data bus input/output connections of the central processing unit and the peripheral (a typical PCI bus of McClear et al.), and control logic (174/ASIC 85, for example) having an input for receiving a CPU chip select signal and an output for providing a peripheral control signal which ends at a preselected time (predetermined time) before the end of the read operation (see at least Fig. 2 and the description thereof), the control logic being connected to a control input of the peripheral and to the output enable input of the transceiver. Applicants disagree with these characterizations of the McClear reference and will address each of them below.

While the transceiver of McClear does have bus hold circuitry, it does not have an output enable input or anything equivalent to such an input. The Examiner referenced Fig. 2 of McClear for support of the existence of an output enable input. In Fig. 2 there are only two input/output terminals, labeled A and B, for the transceiver. These terminals are data lines for connection to the data bus. There are no other inputs or outputs shown in Fig. 2. In particular, there are no control signal inputs or outputs shown in Fig. 2. Therefore, there can be no output enable input.

The control logic 174 does not have an input for receiving a CPU chip select signal or an output for providing a peripheral control signal which ends at a preselected time before the end of the read operation, and the control logic is not connected to a control input of the peripheral or to the output enable input of the

transceiver. Reference to Fig. 2 of McClear shows that the "control logic" 174 is actually a collision arbitration unit which is completely internal to the transceiver. It prevents the output drivers 175 and 176 from operating at the same time. There are no control signal inputs or outputs shown in Fig. 2 and therefore there can be no connection to a peripheral control input or to an output enable input of the transceiver. The only peripheral shown in McClear is the ASIC 85 in Fig. 5 which has only one connection to the transceiver 83, i.e. the data connection B. Since the collision arbitration unit is part of the transceiver, it cannot have a connection to an input of the transceiver, i.e. it is already in the transceiver.

With regard to Claim 6, the Examiner asserts that McClear et al. discloses a buffer (shown generally at 0-N Fig. 5; see also Fig. 3, particularly) connected between an address output of said central processing unit and an address input of said peripheral device, said buffer having an output enable input connected to a chip select signal.

Reference to Fig. 5 and the description of Fig. 5, at Col. 9, lines 31-50, clearly shows that McClear does not discuss address signals, address inputs or address outputs. McLear states that the ASIC 85 sends and/or receives data, at lines 36-37. At lines 39-40, it is stated that "the transceiver circuit 83 will detect any new data on either the A or B port and transmit it to the other port." There is no output enable input and no chip select signal shown or even suggested by McClear.

With regard to Claim 7, the Examiner asserts that "the preselected time (predetermined time) is equal to or greater than the maximum time to enable high impedance state of said transceiver. In other words, active output will remain for a predetermined time period before returning to a tri-state or high impedance state." The Examiner did not identify specific support for this in McClear.

Claim 7 calls for a time period having a length equal to or greater than the maximum time to enable high impedance state of the transceiver, with the time period ending at the end of the read operation. McClear provides no teaching concerning placing the outputs of a transceiver into the high impedance state at a time related to the end of a read operation. McClear does not mention a preselected or predetermined time relative to a read cycle. At Col. 3, lines 45-60, McClear teaches that "Transition detection circuitry 173 and 179 also provide a timed output signal to the drivers 176 and 175, so that the drivers are only enabled for the time required to bring the receiving bus to a stable data value. After that time has elapsed, the active driver is disabled by the transceiver device and the data value is maintained by the bus holder circuitry 171 or 177. ... the data transmission is timed so that the output drivers are active for as short a time as possible while maintaining data integrity." Further references to this time period are found at: Col. 5, lines 19-29; Col. 6, lines 29-32; Col. 8, lines 8-10, Col. 9, lines 1-7; and Col. 10, lines 29-31. This time period begins with the

occurrence of a data transition and ends as soon as possible afterwards. It has nothing to do with the end of a read operation.

With regard to Claims 1-3 and 9, the Examiner asserts that it is clear that one using the apparatus of McClear et al. would have performed the same steps set forth in Claims 1-3 and 9. As discussed above, the Apparatus of McClear does not have many of the elements of the present invention. As a result, it is impossible for the apparatus of McClear to perform the steps of Claims 1-3 and 9.

The teachings of McClear clearly show that this reference is not applicable to the present invention. At Col. 9, lines 42-50, McClear teaches, that:

"Because the transceiver circuitry will immediately transfer data from one port to the other, it is important that the system be one where it is known when data will be transmitted by the various devices, so that no bus clashing occurs. This is typically the case. For example, in Fig. 5 microprocessor 81 might send out a read request to ASIC 85. Once the request is sent, the microprocessor knows data is expected back from the ASIC 85 device and therefore will not put data out on the bus until the read data is received."

However, as taught by the present Applicants, even after the data is read, there can be a problem of contention if the read operation if followed by a write operation. An implication of McClear, when combined with this teaching, may be

that the CPU should wait before writing data onto the bus. However, that would slow down the system and waste a benefit of a high speed CPU.

In view of the fact that the McClear reference lacks several basic elements of the invention of Claims 1-3, 5-7, 9 and 11 as discussed above, the Applicants submit that these claims are allowable in view of the McClear reference.

Argument re 103 rejections:

Claim 4 and 8 were rejected as being obvious over McClear. The Examiner asserts that McClear discloses the claimed invention including the preselected time (predetermined time). However, McClear et al. does not disclose that the preselected time (predetermined time) is greater than 50 nanoseconds. The Examiner asserts that this time period would be obvious as being only an optimum or workable range.

Claims 4 and 8 cover time periods which end at the end of a read operation. As noted above, the only time period discussed by McClear is a period "as short as possible" which begins upon a transition on the data bus. McClear provides no teaching of any control signal changing the state of a transceiver, much less a control signal changing the state of the transceiver at a time based on the end of a read cycle.

Claim 10 and 12 were rejected as being obvious over McClear for essentially the same reasons a Claims 4 and 8.

Claims 10 and 12 are similar to Claims 4 and 8, except that they provide for the time period to be selected in terms of clock cycle periods. For a read operation which occurs during eight clock cycles, these claims call for changing the state of the transceiver one and one-half cycles before the end of the read operation. The only time period discussed by McClear is a period "as short as possible" which begins upon a transition on the data bus. McClear provides no teaching of any control signal changing the state of a transceiver, much less a control signal changing the state of the transceiver at a time, i.e. clock cycle, based on the end of a read cycle.

In view of these substantial differences between the present invention and the teachings of McClear, the Applicants submit that Claims 4, 8, 10 and 12 are allowable in view of the cited reference.

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CONCLUSION

In view of the above arguments the Applicants respectfully request that the final rejection of the claims be reversed and the case advanced to issue.

The Commissioner is hereby authorized to charge payment of any further fees associated with any of the foregoing papers submitted herewith, or to credit any overpayment thereof, to Deposit Account No. 21-0765, Sprint.

Respectfully submitted,
CONLEY ROSE, P.C.

Date: December 21, 2004

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(VIII) CLAIMS APPENDIX

1. (Previously Presented) A method for preventing contention on a data bus connecting a central processing unit and a peripheral device when the central processing unit calls for a read operation followed by a write operation, comprising:

connecting a transceiver with bus hold circuitry and an output enable input in the data bus between the central processing unit and the peripheral,

generating a control signal which ends at a preselected time before the end of the read operation, and,

providing the control signal to an input of the peripheral and to the output enable input of the transceiver.

2. (Original) The method of Claim 1 further including;

connecting a buffer having an output enable input between an address output of said central processing unit and an address input of said peripheral device, and

providing a chip select signal to the output enable input of said buffer.

3. (Original) The method of Claim 1 wherein said preselected time is equal to or greater than the maximum time to enable high impedance state of said transceiver.

4. (Original) The method of Claim 1 wherein said preselected time is greater than fifty nanoseconds.

5. (Previously Presented) Apparatus for preventing contention on a data bus connecting a central processing unit and a peripheral device when the central processing unit calls for a read operation followed by a write operation, comprising:

a transceiver with bus hold circuitry and an output enable input connected between the data bus input/output connections of the central processing unit and the peripheral, and

control logic having an input for receiving a CPU chip select signal and an output for providing a peripheral control signal which ends at a preselected time before the end of the read operation,

said control logic output connected to a control input of the peripheral and to the output enable input of the transceiver.

6. (Previously Presented) The apparatus of Claim 5, further including;

a buffer connected between an address output of said central processing unit and an address input of said peripheral device, said buffer having an output enable input connected to the chip select signal.

7. (Original) The apparatus of Claim 5 wherein said preselected time is equal to or greater than the maximum time to enable high impedance state of said transceiver.

8. (Original) The apparatus of Claim 5 wherein said preselected time is greater than fifty nanoseconds.

9. (Previously Presented) A method for controlling the reading of data by a processing unit from a peripheral device over a bidirectional data bus during a read operation, said peripheral device having a maximum time to enable high impedance state, comprising;

connecting a transceiver with bus hold circuitry and an output enable input in the data bus between the central processing unit and the peripheral,

generating a peripheral control signal which ends at a time equal to or greater than said maximum time to enable high impedance state before the end of the CPU read command, and,

providing the peripheral control signal to an input of the peripheral and to the output enable input of the transceiver.

10. (Original) The method of Claim 9, wherein said read operation occurs during eight clock cycles and said peripheral control signal ends one and one-half clock cycles before the end of the read operation.

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11. (Original) Apparatus for controlling the reading of data by a processing unit from a peripheral device over a bidirectional data bus during a CPU read operation, said peripheral device having a control input and a maximum time to enable high impedance state, comprising;

a transceiver with bus hold circuitry connected between the data bus input/output connections of the central processing unit and the peripheral, said transceiver having an output enable input,

control logic having an input for receiving a CPU data strobe signal and an output for providing a peripheral control signal which ends at a time equal to or greater than said maximum time to enable high impedance state before the end of the read operation, and,

said control logic output connected to a control input of the peripheral and to the output enable input of the transceiver.

12. (Original) The apparatus of Claim 11 wherein said read operation occurs during eight clock cycles and said peripheral control signal ends one and one-half clock cycles before the end of the read operation.